IN THE CLAIMS – (clean version):

A2

1. (amended) A semiconductor device, comprising:

a logic circuit, which includes a MOS transistor, and

a bias voltage supply circuit, comprising no more than two transistors, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the MOS transistor.

2. The semiconductor device of Claim 1, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

3. The semiconductor device of Claim 2, wherein the MOS transistor of the logic circuit is connected to the first voltage supply line.

4. The semiconductor device of Claim 3, wherein the MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor are PMOS transistors.

5. The semiconductor device of Claim 4, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line.

6. The semiconductor device of Claim 1, wherein the first bias voltage is lower than the second bias voltage.

7. The semiconductor device of Claim 1, further including at least one additional logic circuit coupled to the bias voltage supply circuit.

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8. (amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential; and

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a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor.

9. The semiconductor device of Claim 8, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor.

10. The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the second bias voltage.

11. The semiconductor circuit of Claim 8, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor.

12. (amended) The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the supply line voltage.

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13. (amended) The semiconductor circuit of Claim 8, wherein the bias voltage supply circuit includes a third MOS transistor connected between a first voltage supply line and a bias voltage supply line and a fourth MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

14. (amended) The semiconductor circuit of Claim 13, wherein the first MOS transistor of the logic circuit is connected to the first voltage supply line.

15. (amended) The semiconductor circuit of Claim 14, wherein the first MOS transistor of the logic circuit and the [first] third MOS transistor and fourth MOS transistor are PMOS transistors.

16. The semiconductor circuit of Claim 15, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line.

17. (amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential;

A5 a first bias voltage supply circuit, comprising no more than two transistors, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor; and

a second bias voltage supply circuit, comprising no more than two transistors, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor.

18. The semiconductor device of Claim 17, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor.

19. The semiconductor circuit of Claim 17, wherein the first bias voltage from the first bias supply circuit is lower than the second bias voltage from the first bias supply circuit.

20. The semiconductor circuit of Claim 17, wherein the first bias voltage from the second bias supply circuit is lower than the second bias voltage from the second bias supply circuit.

21. The semiconductor circuit of Claim 17, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor.

22. The semiconductor circuit of Claim 17, wherein the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

A6 23. (amended) The semiconductor circuit of Claim 17, wherein the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a second MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line.

24. The semiconductor circuit of Claim 17, wherein:

the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor; and

the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a third bias supply line.

25. The semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors.

26. The semiconductor circuit of Claim 23, wherein the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors.

27. The semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors and the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors.

REMARKS

Applicants submit a separate letter in which Applicants propose adding the legend "(PRIOR ART)" to drawing figures 8 and 9, as requested by the Examiner. Applicants respectfully request approval.

By this amendment the minor informality in the Abstract identified by the Examiner has been corrected. Similarly, a new title of the invention is submitter herewith, as requested by the Examiner.